VERSION WITH MARKINGS TO SHOW CHANGES MADE IN THE SPECIFICATION

Page 2, line 3 to page 3, line 9 have been amended as follows:

Integrated circuits commonly use multilevel interconnections as a means for electrically interconnecting semiconductor devices which include active or passive circuit elements. High-density integrated circuits such as Dynamic Random Access Memories (DRAMs) or Static Random Access Memories (SRAMs) are typically comprised of hundreds of thousands or millions of semiconductor devices on a silicon substrate. These high density integrated circuits can be manufactured using a Complementary Metal-Oxide Semiconductor (CMOS) process and typically involve the use of multiple layers of vertically stacked metal interconnects. Fabrication of CMOS integrated circuits typically involves many manufacturing steps which include repeated deposition or growth, patterning, and etching of thin films of semiconductor, polysilicon, metal, and dielectric materials to form the electrical circuitry which typically consists of n-channel and p-channel transistors and active and passive circuit elements. Typically, the steps to form the n-channel and p-channel transistors are completed before the interconnect metal is formed. While active and passive circuit elements may be fabricated at any time during the processing sequence depending on the particular type of element, active circuit elements such as magnetoresistive memory storage bits are typically fabricated at the third metal level after the n-channel and p-channel transistors are formed.

Forming metal interconnect typically requires the repeated steps of deposition or growth, patterning, and etching of metal, via and dielectric layers as necessary to connect the integrated circuit elements. Typically, after the n-channel and p-channel transistors have been patterned and etched, a dielectric layer (e.g., silicon oxide) is formed over the surface of the topography to provide dielectric isolation between the devices and the overlying interconnect conducting regions. Next, a contact layer is **[next]** patterned into the dielectric layer to define openings in the dielectric layer where ohmic contacts will interconnect a first level of metal to the source, drain and gate regions of the n-channel and p-channel transistors. The contact layer patterning is accomplished by first depositing a photoresist layer over the dielectric layer. The photoresist is next selectively exposed to light through a patterned reticle having the desired layer pattern. After exposure, the photoresist is developed to form a resist mask for the desired layer pattern.

The exposed layer is then etched to define the contact openings. The last step is to deposit and etch the contact metal.

Page 4, lines 11-17 have been amended as follows:

As successive metal interconnect layers are fabricated to interconnect magnetoresistive bits, smooth planar surfaces become increasingly difficult to maintain. The resulting uneven topographies create a variety of problems, all of which reduce integrated circuit functional yields and reliability. One problem that results is that photoresist material cannot be applied in a uniform fashion over uneven topographies. Thus, when the steps of patterning the photoresist to form a resist mask and etching the exposed layer occur, features of the exposed layer may not be completely etched due to the incomplete development of the photoresist.

Page 7, line 6 to page 8, line 4 have been amended as follows:

In a preferred embodiment of the present invention, an initial dielectric layer is formed to overlie a semiconductor substrate. Next, the initial dielectric layer is planarized using a chemical mechanical polish. A magnetoresistive storage layer is then formed to overlie the initial dielectric layer. The magnetoresistive storage layer may be comprised of a variety of magnetic materials including materials used to form Anisotropic Magnetoresistance (AMR) devices, Giant Magnetoresistance (GMR) devices, Colossal Magnetoresistance (CMR) devices, Tunneling Magnetoresistance (TMR) devices, Extraordinary Magnetoresistance (EMR) devices or Very Large Magnetoresistance (VLMR) devices. In a preferred embodiment, the magnetoresistive storage layer is formed of materials which form "pseudo" spin valve structures. Next, an initial stop layer is formed to overlie the magnetoresistive storage layer. A final stop layer is then formed to overlie the initial stop layer. A hardmask layer is next formed to overlie the final stop layer. The hardmask layer and the final stop layer are etched until the initial stop layer is exposed to define an etch region. Using the etch region as an etch opening, the initial stop layer and the magnetoresistive storage layer are etched using blanket ion milling until the initial dielectric layer is exposed to define two or more magnetoresistive memory storage bits. An isolation layer having sufficient thickness to fill in the gaps created by etching the etch region is formed over the hardmask layer and in the etch region. The isolation layer is planarized using a chemical mechanical polish until regions of the final stop layer are exposed. The interconnect layer is then formed over the exposed regions of the final stop layer and is patterned and etched to electrically interconnect at least two magnetoresistive memory storage bits.

Page 9, lines 2-5 have been amended as follows:

Other objects of the present invention and many of the attendant advantages of the present invention will be readily appreciated as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, in which like reference numerals designate like parts throughout the figures thereof, and wherein:

Page 9, line 20 to page 10, line 15 have been amended as follows:

FIG. 1 is cross-sectional view showing **an** initial dielectric layer 14 deposited to overlie a semiconductor substrate 12. It is possible for many types of materials or structures to be formed on substrate 12 prior to forming initial dielectric layer 14, including contact, via or interconnect metallization layers, CMOS integrated circuits, or active or passive circuit elements. Fabrication of CMOS integrated circuits typically involves the repeated deposition or growth, patterning, and etching of semiconductor, polysilicon, metal, or dielectric materials to form electrical circuitry which may include n-channel and p-channel transistors. These transistors, along with the contact, via or interconnect metallization layers, may form complex circuit functions which are required to operate a magnetoresistive memory and further may include such functions as read and write control. The exact composition of the materials or structures formed on substrate 12 does not directly affect the practice of the present invention.

Initial dielectric layer 14 is a dielectric material such as silicon nitride which is deposited on the surface of substrate 12. Dielectric layer 14 is planarized using a chemical mechanical polish to a degree of flatness which is sufficient for **a** magnetoresistive layer 16. Once planarized, dielectric layer 14 provides the uniform surface required by the very thin films used to form magnetoresistive layer 16.

Page 11, lines 3-19 have been amended as follows:

FIG. 3 is a cross-sectional view showing **an** initial stop layer 18, **a** final stop layer 20 and **a** hardmask layer 22 formed over the magnetoresistive layer 16. The exact composition of initial stop layer 18 does not directly affect the practice of the present invention, except that it must be electrically conductive. **[The initial] Initial** stop layer 18 may include any materials having an etch selectivity which is greater than the etch selectivity of the hardmask layer 22 and final stop layer 20. In exemplary embodiments, these materials may include chromium and silicon.

[The final] **Final** stop layer 20 is deposited to overlie initial stop layer 18. The exact composition of final stop layer 20 does not directly affect the practice of the present invention, but may include any materials that are electrically conductive, inert to chemicals contained in polishing slurries, and having a chemical mechanical polish selectivity which is greater than the chemical mechanical polish selectivity of the hardmask layer 20. In exemplary embodiments, these materials may include titanium and tungsten.

[The hardmask] **Hardmask** layer 22 is deposited to overlie final stop layer 20. The exact composition of hardmask layer 22 does not directly affect the practice of the present invention. In exemplary embodiments, this material may be silicon dioxide.

Page 12, lines 10-15 have been amended as follows:

[Initial] **An initial** isolation **or dielectric** layer 24 is deposited to overlie the hardmask layer **22** and the plurality of etch regions defined by blanket ion milling.

FIG. 6 is a cross-sectional view showing **[the]** **a** final isolation layer 26 deposited to overlie initial isolation layer 24. The thickness of **[the]** final isolation layer 26 must be great enough to fill any gaps created by etching the etch region.

Page 13, lines 1-6 have been amended as follows:

FIG. 8 is a cross-sectional view showing the structure after **an** interconnect layer 28 has been deposited to overlie final stop layers 20a and 20b, initial isolation layer 24 and final isolation layer 26. Interconnect layer 28 has been etched to form a plurality of interconnect regions which connect each of the plurality of magnetoresistive elements to each other. The actual composition of the interconnect layer does not directly affect the practice of the present **[device]** **invention**, but may include any materials which provide a conductive interconnect between the magnetoresistive elements.

Page 14, lines 5-17 have been amended as follows:

FIG. 9 is a cross-sectional diagram showing one of a plurality of embodiments of a magnetoresistive storage bit. **[The figure]** **FIG. 9** illustrates the generalized components of magnetoresistance layer 16, which is composed of dual magnetic layers 30a and 30b and a coupling layer 30c.

FIG. 10 **[is a figure illustrating]** **illustrates** the read and write control circuitry coupled to an array of magnetoresistive memory storage bits 36a. The plurality of magnetoresistive storage bits 36a are connected by **[the]** **a** plurality of interconnects 36b to form a bit string 36.

The address of the memory location is determined by selection of both **[the]** **a** word line 32 and **[the]** bit string 36.

The present invention may be embodied in other specific forms without departing from the spirit or essential attributes thereof**[, and it]**. **It** is therefore desired that the present embodiment be considered in all respects as illustrative and not restrictive, reference being made to the appended claims rather than to the foregoing description to indicate the scope of the invention.

IN THE ABSTRACT

Page 35, lines 2-13 have been amended as follows:

A process **[of forming]** **forms** electrical interconnects between memory bits in a magnetoresistive memory device. **[A]** **An initial** dielectric layer is formed to overlie a semiconductor substrate. A magnetoresistive storage layer is formed over the **initial** dielectric layer. An electrically conductive stop layer that is selective to etch processes and is mechanically hard is deposited over the magnetoresistive **storage** layer. A hardmask layer is formed to overlie the stop layer. The hardmask layer is etched to expose the stop layer. The stop layer and the magnetoresistive **storage** layer are etched using ion milling until the initial dielectric layer is exposed, defining individual magnetoresistive memory bits. **[A dielectric]** **An isolation** layer is formed over the hardmask layer and in the etch regions between magnetoresistive bits. The **[dielectric]** **isolation** layer is planarized using chemical mechanical polish (CMP) until the stop layer is exposed. An interconnect layer is then formed over the exposed regions of the stop layer and is etched to form electrical interconnects between memory bits.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0661.

TMM

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